## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claims 1-20 (canceled).

21. (Presently Amended) A method of fabricating a mask read only memory, comprising:

forming a gate insulation layer over a semiconductor substrate;

forming a first polysilicon layer over the gate insulation layer;

forming photoresist patterns over the first polysilicon layer, which entirely cover a peripheral circuit region but are patterned in a cell array region to expose regions that are to become buried impurity diffusion regions;

performing ion implantation using the photoresist patterns as a mask to form a plurality of buried impurity diffusion regions near the surface of the semiconductor substrate, wherein the buried impurity diffusion regions are formed in parallel, are separated from each other by a first predetermined interval, and extend in the same direction;

removing the photoresist patterns, and sequentially stacking a second ~~silicon~~ polysilicon layer and a metal silicide layer over the first polysilicon layer; and

sequentially etching the first and second polysilicon layers and the metal silicide layer so as to form a plurality of word lines, wherein the word lines are formed in parallel, are separated from each other by a second predetermined interval, and extend in a direction perpendicular to that of the buried impurity diffusion regions.

22. (Original) A method of fabricating a mask read only memory, as recited in claim 21, wherein the buried impurity diffusion regions act as bit lines and as sources/drains of cell transistors.

23. (Original) A method of fabricating a mask read only memory, as recited in claim 21, further comprising doping first and second polysilicon layers with $POCl_3$ ions so as to provide conductivity to the first and second polysilicon layers.

24. (Original) A method of fabricating a mask read only memory, as recited in claim 21, wherein the gate insulation layer is formed to a thickness of about 50-150 Å, the first polysilicon layer is formed to a thickness of about 100-1000 Å, the second polysilicon layer is formed to a thickness of about 500-1500 Å, and the metal silicide layer is formed to a thickness of about 500-2000 Å.

25. (New) A method of fabricating a mask read only memory, comprising:

forming a gate insulation layer over a semiconductor substrate;

forming a plurality of conductive layer patterns over the gate insulation layer, the conductive layer patterns being formed in parallel, being separated from each other by a first predetermined interval, and extending in the same direction;

performing ion implantation, using the conductive layer patterns as a mask, to form buried impurity diffusion regions in an exposed region of the semiconductor substrate between the conductive layer patterns;

forming a conductive layer over the conductive layer patterns and the buried impurity diffusion regions; and

etching the conductive layer and the conductive layer patterns to form a plurality of word lines and a plurality of pad conductive layers,

wherein the word lines are formed in parallel, are separated from each other by a predetermined interval, and extend in a direction perpendicular to the buried impurity diffusion regions,

wherein channel regions are defined by the areas between the buried impurity diffusion regions that are overlapped by the word lines, and

wherein the pad conductive layers are formed to have an island shape in the channel regions, and form ohmic contacts with the word lines.

26. (New) A method of fabricating a mask read only memory, as recited in claim 25, wherein the forming of the buried impurity diffusion regions comprises:

implanting impurity ions at a low concentration into the semiconductor substrate using the conductive layer patterns as a mask, to form low-concentration buried impurity diffusion regions that are self-aligned with the conductive layer patterns;

simultaneously forming spacers on the sidewalls of the conductive layer patterns and removing exposed portions of the gate insulation layer, so as to partially expose the low-concentration buried impurity diffusion regions; and

implanting impurity ions at a high concentration into the semiconductor substrate, using the conductive layer patterns and the spacers as a mask, to form high-concentration buried impurity diffusion regions in the low-concentration buried impurity diffusion regions.

27. (New) A method of fabricating a mask read only memory, as recited in claim 26, wherein in the high-concentration impurity implantation, arsenic (As) ions are implanted at an energy of about 40 keV to a dose of about $5.0 \times 10^{15}$ ions/cm$^2$.

28. (New) A method of fabricating a mask read only memory, as recited in claim 26, further comprising oxidizing the exposed surface of the semiconductor substrate to form grown insulation layers over the surface of the high-concentration buried impurity diffusion regions.

29. (New) A method of fabricating a mask read only memory, as recited in claim 28, wherein the grown insulation layers are formed to a thickness of about 100-1000Å.

30. (New) A method of fabricating a mask read only memory, as recited in claim 25, wherein the forming of the conductive layer patterns comprises:

forming a conductive material layer over the gate insulation layer;

forming an etch mask layer on the conductive material layer;

forming spacers on the sidewalls of the etching mask layer; and

etching the conductive material layer using the etching mask layer and the spacers as an etching mask to form the conductive layer patterns,

wherein the forming of the buried impurity diffusion regions comprises implanting impurities over the entire surface of the resultant structure using the etch mask layer, the spacers, and the conductive layer patterns as a mask, to form buried impurity diffusion regions in an exposed region of the semiconductor substrate.

31. (New) A method of fabricating a mask read only memory, as recited in claim 30, further comprising, after the forming of the buried impurity diffusion regions, oxidizing the exposed surface to the semiconductor substrate to form grown insulation layers over the surface of the buried impurity diffusion regions.

32. (New) A method of fabricating a mask read only memory, as recited in claim 31, wherein the grown insulation layers are formed to have a thickness of about 100-1000Å.

33. (New) A method of fabricating a mask read only memory, as recited in claim 25, wherein the pad conductive layers comprise a material capable of forming the ohmic contacts with the word lines.

34. (New) A method of fabricating a mask read only memory, as recited in claim 33, wherein the pad conductive layers comprise polysilicon, and the words lines comprise a polycide layer in which a polysilicon layer and a metal silicide layer are stacked.